Claims

What is claimed is:

1. A memory system, comprising:

a programmable storage device to store one or more indicators;

cache tag logic; and

a control circuit coupled to the storage device and to the cache tag logic, the control circuit to receive data and to determine, based on the one or more indicators, whether to update the cache tag logic to track the data.

2. The memory system of Claim 1, and further including a cache coupled to the cache tag logic to store the data, and wherein the control circuit further includes circuits to determine, based on the one or more indicators, whether to store the data to the cache.

3. The memory system of Claim 2, wherein one of the indicators indicates the cache is not available for use.

4. The memory system of Claim 2, and further including:

at least one requester coupled to the control circuit to request data from, and store data to, the cache;

a main memory to provide to the cache requested data that is not stored within the cache; and

wherein the control circuit includes a circuit that may replace the data in the cache based on the state of the indicators.

5. The memory system of Claim 4, wherein the main memory provides data to the cache in response to a request that is any one of multiple request types, wherein at least one of the indicators identifies one or more of the request types, and wherein the control circuit prevents the replacement of the data in the cache if the data was provided in response to any of the identified request types.

6. The memory system of Claim 4, wherein the one or more request types includes a request type indicating the data will be modified by a requester.

7. The memory system of Claim 4, wherein at least one of the indicators identifies one or more of the at least one requester, and wherein the control circuit replaces the data in the cache if the data was returned from the main memory in response to a request issued by any of the identified requesters.

8. The memory system of Claim 4, wherein the main memory provides data to the cache with a response that is any one of multiple response types, wherein at least one of the indicators identifies one or more of the response types, and wherein

the control circuit replaces the data in the cache if the data is returned from the main memory with any of the identified response types

9. The memory system of Claim 2, and further including at least one requester coupled to the control circuit to return data to the cache tag logic, and wherein the control circuit determines whether to store the returned data to the cache based on the state of at least one of the indicators.

10. The memory system of Claim 9, wherein the at least one requester returns data to the cache tag logic during an operation that is any one of multiple operation types, wherein the indicators include an indicator to identify one or more of the operation types, and wherein the control circuit stores the returned data to the cache if the returned data is returned during any of the identified operation types

11. The memory system of Claim 10, wherein the control circuit is further adapted to store the returned data to the cache based, at least in part, on whether a cache hit occurred.

12. The memory system of Claim 9, and further including a main memory coupled to the control circuit, and wherein the control circuit is adapted to forward the returned data to the main memory based, at least in part, on the state of at least one of the indicators.

13. The memory system of Claim 12, wherein memory coherency actions may be incomplete for the returned data or for associated data retained by the at least one requester or the cache, and further including a request tracking circuit coupled to the control circuit to prevent the returned data from being forwarded to the main memory until all of the memory coherency actions have been completed for the returned data or for the associated data.

14. The memory system of Claim 1, wherein the programmable storage device includes circuits to store microcode, and wherein the control circuit is controlled by the microcode..

15. The method of Claim 1, and further including mode switch logic coupled to the programmable storage device to automatically re-program at least one of the indicators in response to monitored conditions occurring within the memory system.

16. A method of controlling a memory system having cache tags and one or more programmable control indicators, comprising:

a.) obtaining data; and

b.) determining whether to update the cache tags to record the data based on the state of one or more of the control indicators.

17. The method of Claim 16, wherein the memory system includes a cache, and further including determining whether to store the data in the cache based on the state of one or more of the control indicators.

18. The method of Claim 17, wherein the memory system includes a main memory coupled to the cache tags, and wherein the obtaining step includes:

providing a request for the data to the main memory; and

receiving the data from the main memory.

19. The method of Claim 18, wherein the request is any one of multiple types, wherein one of the control indicators identifies one or more of the multiple request types, and wherein at least one of the determining steps is performed based, at least in part, upon whether the request is any of the identified response types.

20. The method of Claim 18, wherein the data is provided from the main memory with a response type that is any one of multiple response types, wherein one of the control indicators identifies one or more of the multiple response types, and wherein at least one of the determining steps is performed based, at least in part, upon whether the request is any of the identified response types.

21. The method of Claim 18, wherein the memory system is coupled to at least one requester, wherein one of the control indicators identifies one or more of the at least one requester, and wherein at least one of the determining steps is performed

based, at least in part, upon whether the request was initiated by any of the identified requesters.

22. The method of Claim 17, wherein the memory system is coupled to at least one requester, and wherein step a.) includes obtaining the data from any one of the at least one requester.

23. The method of Claim 22, wherein the data is obtained during an operation that is any of multiple operation types, wherein one of the control indicators identifies one or more of the operation types, and wherein at least one of the determining steps is based, at least in part, on whether the data is obtained during any of the identified operation types.

24. The method of Claim 23, wherein at least one of the determining steps is based, at least in part, on whether a cache hit occurs.

25. The method of Claim 22, wherein the memory system includes a main memory, and further including providing the data to the main memory instead of storing the data into the cache.

26. The method of Claim 25, wherein the data is associated with incomplete memory coherency actions, and further including preventing the data from being

provided to the main memory until all incomplete memory coherency actions have been completed.

27. The method of Claim 16, and further comprising:

c.) monitoring conditions within the memory system; and

d.) automatically re-programming at least one of the control indicators based on one or more of the monitored conditions.

28. A memory system, comprising:

main memory means for storing data;

cache means for storing a subset of the data; and

programmable storage means for storing control indicators to select the subset of the data.

29. The memory system of Claim 28, wherein requests are issued to the main memory to retrieve data from the main memory, and wherein the programmable storage means includes means for selecting the subset of the data based, at least in part, on a type of request that was issued to retrieve the subset of the data from the main memory.

30. The memory system of Claim 28, and further including one or more requester means for causing data to be retrieved from the main memory, and wherein the programmable storage means includes means for selecting the subset of the data

based, at least in part, on the identify of one or more of the requester means that caused data to be retrieved from the main memory.

31. The memory system of Claim 28, wherein the main memory means includes means for returning a response type to the cache means with data, and wherein the programmable storage means includes means for selecting the subset of the data based, at least in part, on the response type.

32. The memory system of Claim 28, and further including requester means for returning data to the cache means, and wherein the programmable storage means includes means for selecting whether data returned by the requester means will be stored to the cache means.

33. The memory system of Claim 32, wherein the requester means includes means for returning data during any of multiple types of operations, and wherein the programmable storage means includes means for selecting whether returned data will be stored to the cache means based, at least in part, on the type of operation that resulted in return of the data.

34. The memory system of Claim 32, wherein the programmable storage means includes means for selecting whether data returned by the requester means will be stored to the cache means based, at least in part, on whether a cache miss occurred to the cache means.

35. The memory system of Claim 28, and further including mode switch means for modifying the state of one or more of the control indicators based on monitored conditions occurring within the memory system.

36. The memory system of Claim 28, and wherein the cache means includes cache tag means for tracking data that may be stored to the cache means, and wherein the programmable storage means includes means for determining whether to update the cache tag means to track data.

37. The memory system of Claim 36, wherein the programmable storage means includes means for enabling the tracking by the cache tag means of predetermined data that is not included in the subset of the data stored within the cache means.